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ENHANCED AC-TO-AC FREQUENCY CHANGER BASED ON MULTI-PHASE SMART COMPARATIVE COMMUTATION

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ABSTRACT

Direct AC to AC power conversion was always a challenge to be proposed as an alternative for the DC-link one. This is due to multiple of reasons such as less complexity, power regeneration, and unity power factor privileges. However, the challenge is represented by producing a direct AC to AC system with output waveforms having reduced total harmonic distortion comparable or superior to that generated by the DC-link converters. In such a trend this paper introduces an enhanced AC-to-AC frequency changer with reduced total harmonic distortion frequency spectrum compared to the envelope cycloconverter one. This proposed work introduces smart comparative phases switching carried out via a processing unit that detects and measure the analogue voltages of each phase and sends a switching triggers to the power switching circuit. The proposed work reflected an effective reduction in output waveforms harmonic content (about 60%) compared to the envelope cycloconverter with low cost system requirements.

KEYWORDS: A. C. Converters, Cyclo Converters, Frequency Changers, Power Electronics

INTRODUCTION

Many researches were carried out in performing frequency converters to satisfy the phase and harmonic requirements. Cycloconverters might be the simplest method of obtaining a “divide-by” fundamental harmonic component. Envelope Cycloconverter output waveform fundamental component has the privilege of being the dominant and first harmonic component in the frequency spectrum [1]. Other converters than cycloconverter suffer from added conversion processes and added DC-link step which requires a large capacitors and may reflect problems experienced in a short circuit [2]. However, the ordinary cycloconverter output waveforms still suffering from high harmonic content with respect to the desired fundamental component within the frequency spectrum which was proved analytically by many researches [3, 4]. Moreover, trends also available to merge between the cycloconverter and the inverter referred as hybrid cycloconverter which are capable of improving the performance of the standard cycloconverter by adding an auxiliary forced commutated inverter [5].

In envelope cycloconverters, the output waveform will result in (N) number of positive supply half cycles driven by the Positive –converter and the same number of the negative supply half cycles driven by the Negative-converter to form a periodic output sinusoidal load voltage with frequency equal to:

$$f_0 = \frac{\text{SupplyFrequency}}{\text{numberof totalsupply waveforms injected}} = \left[\frac{f_{supply}}{N}\right] \quad (1)$$

The supply frequency is taken to be 50Hz or supply periodic time (T) is 20msec. The resulted waveforms suffer from high harmonic contents which makes such converter a bad choice in power applications. The harmonic content is

measure by the well-known factor, the percentage total harmonic distortion (THD%) which is described as;

$$THD\% = \sqrt{\frac{\sum_{n=2}^{\infty} C_n^2}{C_1^2}} \times 100 \quad (2)$$

Where the summation of all harmonic components (C_n) excluding the fundamental one divided by the fundamental harmonic component (C_1). Accordingly, Figure 1 shows the THD% of each fundamental frequency component generation case. Many trends were made to eliminate the weakness of the cycloconverter by focusing on decreasing the level of the THD% using direct methods [6-8].

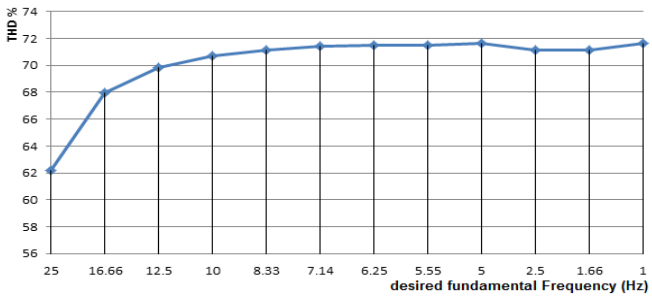
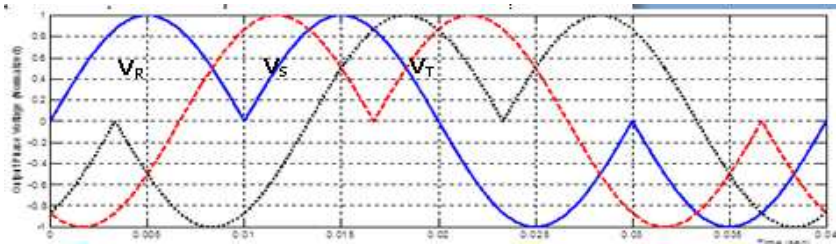


Figure 1: THD% of the Converted Envelope cycloconverter Waveforms

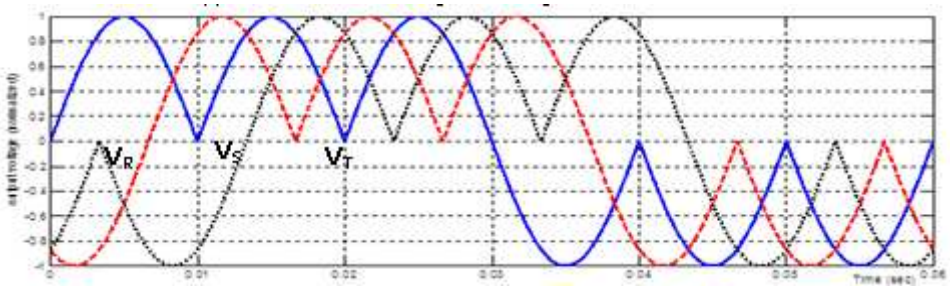
PROPOSED SYSTEM OPERATION PRINCIPLE

The three phase output waveforms of the envelope cycloconverter are shown in Figure 2 for two cases of converting the supply frequency 50Hz to 25 Hz (N=2), and 50Hz to 16.66 Hz (N=3). The two cases were taken for demonstration purposes and the following theory may be applied for any value of divide-by factor (N).

The operation principle of the proposed converter depends on assuming one phase to be the main phase and other phases to be compared to this phase. If V_R is considered as the main output phase, then other phases (V_S and V_T) should be compared to V_R within the comparative period T_C shown in Figure 2.



(a) Converted 25Hz 3-Phase Output Waveform

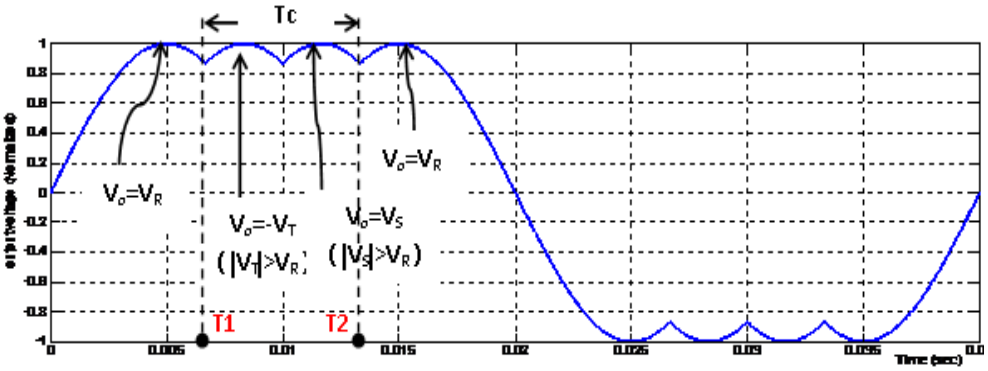


(b) Converted 16.6Hz 3-Phase Output Waveform

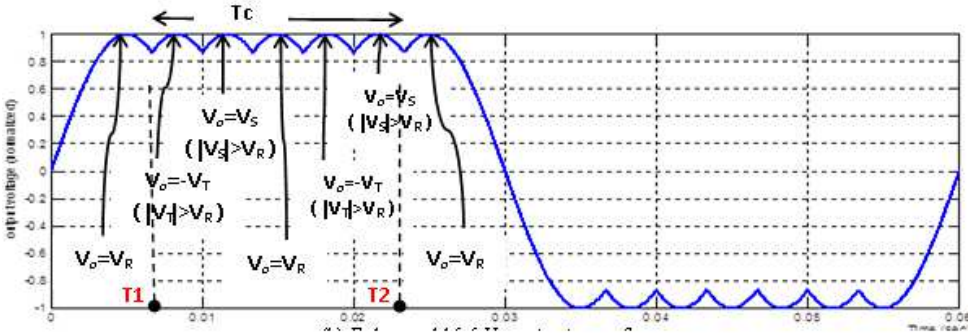
Figure 2: Converted 25Hz and 16.66 Hz 3-phase Waveforms of the Ordinary Envelope cycloconverter

The procedure depends on waveform reforming or shaping of the pre-assumed main phase using smart switching technique. This is done by comparing other phases to the main phase and switching the one with higher level. The comparison is made only within periods of T_C which will lead to multiple switching of portion of phases which have level higher than the main one.

Figure 3 shows the enhancement of the two cases previously presented in Figure 2 after applying the smart switching technique, assuming V_R as the main phase under enhancement. The procedure works within the comparison period T_C and compares the main phase (assumed here V_R) with the absolute value of other phases and switching the higher level phase to the output node.



(a) Enhanced 25Hz Output Waveform



(b) Enhanced 16.6 Hz Output Waveform

Figure 3: Proposed smart switching Enhanced 25Hz and 16.66 Hz output waveforms

THEORETICAL CALCULATIONS

The kernel part in this proposal is smart switching procedure. It is carried out using processing unit based on microprocessor chip and it is responsible on comparison and reselection between phases in certain time. However, this unit firstly needs to predefine some information such as the starting and ending time of each phase voltage and comparison period T_C defined by starting (T1) and ending (T2) times. Based on this defined information this unit can play the rules of switching.

COMPARISON PERIOD FORMULA DERIVATION

This period of time is considered as the most important timing factor, which enable the processing unit to start and stop the comparative switching procedure in both the positive and negative halves of the main phase waveform. Now remembering that the supply periodic time is T, the start of the comparison period is T1 and the end of the comparison

period is T2 as depicted in Figure 3. T1 may be found as the intersection of the first phase (V_R) with the negative of the third phase (V_T), therefore;

$$V_R = -V_T \qquad at \quad t = T1$$

and since;

$$V_R = Sin(\omega T_1) \; and \; V_T = Sin(\omega T_1 - 2 * \frac{2\pi}{3})$$

then; $Sin(\omega T_1) = -Sin(\omega T_1 - \frac{4\pi}{3})$

Taking the inverse sine function for both sides, result in

$\omega T_1 = -(\omega T_1 - \frac{4\pi}{3})$ and since $\omega = \frac{2\pi}{T}$, then;

$$T_1 = \frac{T}{3} \tag{3}$$

where T is the supply periodic time.

The formula shown in equation (3) is derived assuming the phase under enhancement is V_R (master phase). Adding the three phase time relation, the starting comparison time in general is;

$$T_1 = M \frac{T}{3} \tag{4}$$

where M is the phase sequence indicator (1, 2, and 3). Although T may be taken as any supply frequency, calculations in this paper carried out for the 50Hz one (T=0.02sec). Therefore, the equation of finding the starting time of comparison will be:

$$T_1 = M \frac{0.02}{3} \tag{5}$$

Now; it is easy to find the comparison end time in terms of N (Divide-by factor) and M from Figure 3 as;

$$T_2 = 0.01\,N + \frac{0.02}{3} M - \frac{0.04}{3} \tag{6}$$

The start and end time calculations were made for three cases of divide-by factor (N) according to the derived formulas in equations (5) and (6) as in Table (1).

Table 1: Calculated Start and end Comparison Time Values for Different Values of N and M

Divide-by Factor (N)	Phase Number (M)	Comparison Start Time (T_1)	Comparison End Time (T_2)
2	1	0.0066	0.0133
	2	0.0133	0.02
	3	0.02	0.0266
3	1	0.0066	0.0233
	2	0.0133	0.03
	3	0.02	0.0366
4	1	0.0066	0.0333
	2	0.0133	0.04
	3	0.02	0.0466

COMPARATIVE RULES REPRESENTATION

Rules are followed only within the predefined comparison period (T_C) by the processing unit. These rules are very simple and might be described as follows;

The cycloconverter j[th] phase waveform voltage may be described by the following formula according to waveform shown in Figure 4 [1];

$$v_j(\omega t) = \sum_{i=0}^{i=1} \sum_{D=1+iN}^{D=(1+i)N} (-1)^{D+1-i} \sin(\omega N t - \gamma_j) \Big|_{\frac{\gamma_j+(D-1)\pi}{N}}^{\frac{\gamma_j+D\pi}{N}}$$

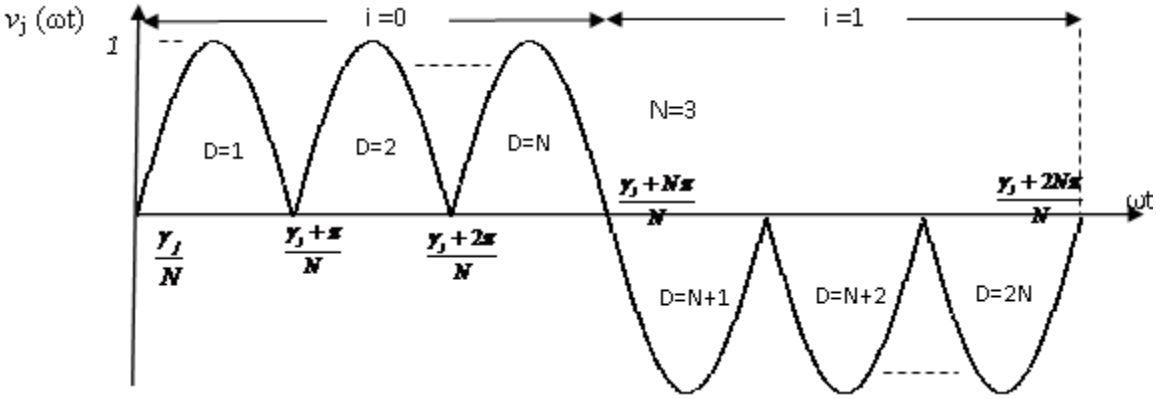


Figure 4: Typical Load Voltage Waveform for Divide by 3 Resistive Load cycloconverter (N=3)[1]

where γ_j is either $0, \frac{2\pi}{3}, or \frac{4\pi}{3}$ and D and i are waveform subsection index. The load voltage V_j (ωt) equals to either V_R (ωt), V_S (ωt), or V_T (ωt) for j= 1, 2, or 3 respectively which represent the three phase cycloconverter output waveforms.

To start the waveform enhancement in order to reduce the relatively high THD% content within these waveforms, rules are created to perform a smart switching process between these three phases and produce another three phase waveforms with lower harmonic content and improved sinusoidal waveform shape. From the waveforms shown in Figures (3) and (4), the following may be deduced:

Positive output half cycle Rule is:

$$V_{oj}(\omega t) = \begin{cases} V_j & \gamma_j \le \omega t \le (\gamma_j + \omega T_1) \\ |V_i| \quad if\ |V_i| > V_j \quad where\ i \neq j & \gamma_j + \omega T_1 < \omega t \le \gamma_j + \omega T_2 \\ V_j & \gamma_j + \omega T_2 < \omega t \le \gamma_j + \omega \frac{NT}{2} \end{cases} \quad (7)$$

While, the negative output half cycle Rule is:

$$V_{oj}(\omega t) = \begin{cases} V_j & \gamma_j + \omega \frac{NT}{2} < \omega t \le \gamma_j + \omega T_1 + \omega \frac{NT}{2} \\ -|V_i| \quad if\ |V_i| > |V_j| \quad where\ i \neq j & \gamma_j + \omega T_1 + \omega \frac{NT}{2} \le \omega t \le \gamma_j + \omega T_2 + \omega \frac{NT}{2} \\ V_j & \gamma_j + \omega T_2 + \omega \frac{NT}{2} \le \omega t \le \gamma_j + \omega NT \end{cases} \quad (8)$$

Equations (7) and (8) indicate that the comparative switching will be increased proportionally with the increase of the divide-by factor (N). Although, these two equations helps the microcomputer processor in switching decision making,

the processor already have information about the start of each phase by inputting the zero crossing signal of each phase. This will exclude the need of (γ_j) factor of each phase in equations (7) and (8).

PROPOSED SYSTEM REPRESENTAION AND SIMULATION

The system consists of two representations; first the power side representation which contains the three phase cycloconverter blocks, controlled bank switching elements, and the isolation transformers, and Second the processing smart switching system representation.

The three phase supply system is a star R-S-T-N supply fed to the cycloconverter producing a corresponding three phase divide-by fundamental frequency output waveforms. Furthermore, this cycloconverter output is to be switched using multiple of transistor switches triggered by a microcomputer signals controlled by a smart switching algorithm to produce the new enhanced divide-by waveforms. The proposed system is shown Figure 5 in a simplified block diagram representation. A MATLAB Simulink software package was used to simulate the power side shown in Figure 5.

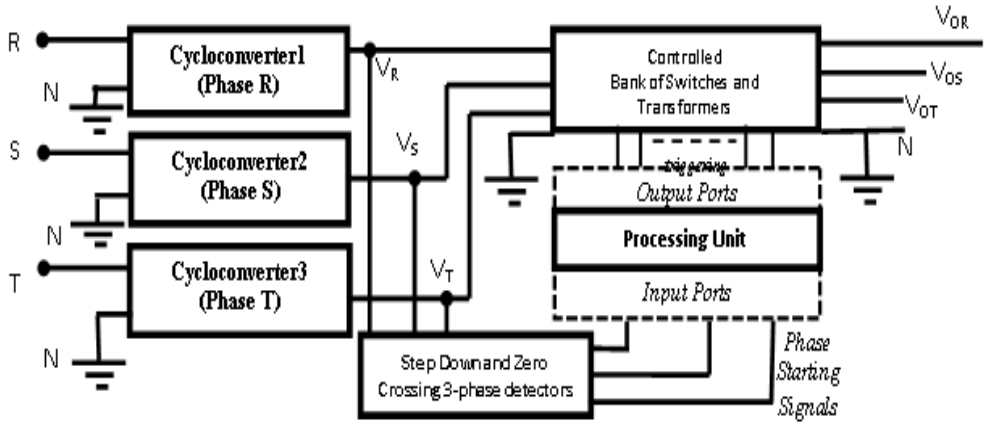


Figure 5: Proposed System Block Diagram

POWER SIDE REPRESENTAION

The three phase power circuit simulation is shown in Figure 6 which shows the enhancement circuit of the divide-by cycloconverter output waveforms. The triggering signals are to be generated by the processing unit to activate the proper bidirectional switch from the controlled bank of switch. Transformers were used as isolation transformers.

The smart switching timing was substituted by triggering circuit for each phase following the rules described in equations (5) and (6) to produce the enhanced waveforms shown earlier in Figure 2 for any value of divide-by factor (N). The three blocks (subsystems) named Cycloconverter1,2, and 3 are the basic envelope cycloconverter circuits. Each subsystem contains the cycloconverter circuit with its corresponding triggering circuit as shown in Figure 7.

SMART SWITCHING PROCESSING UNIT

The smart switching and phase detection are to be simulated using the AT89C52, which is a low power high performance CMOS 8-bit microcontroller with 8k byte flash programmable and erasable read only memory (EPROM) [9]. The three phase instantaneous voltages are reduced to lower level using step down transformer and converted to digital 8-bit word using analogue to digital converter type DC0808 which is compatible to the micro-processor. The clock of the ADC was generated using the NE555 timer connected as an Astable multivibrator.

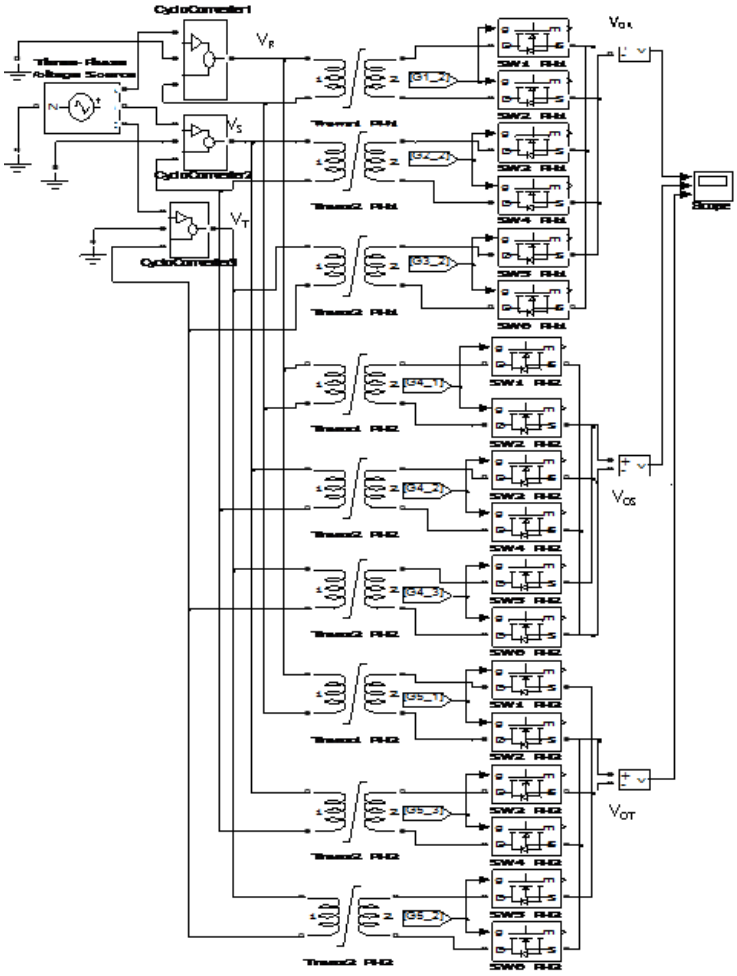


Figure 6: Proposed System Power side Simulink Simulation Circuit

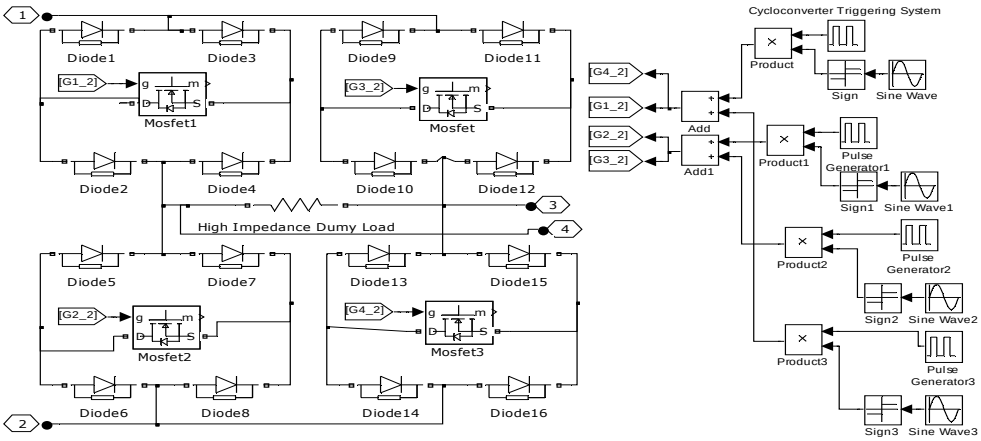


Figure 7: Basic Envelope cycloconverter Simulink simulation circuit (Subsystem)

Moreover, to detect the starting of each cycloconverter output phase waveforms (V_R, V_S, and V_T) for smart switching process, these phases were reduced to lower voltages (5V) using step down transformers and zero-crossing circuits to obtain a corresponding square waveforms. These square waveforms were fed to the microcontroller pre-programmed input pins (AD0, AD1, and AD2) as shown in Figure 8 which represent the simulation of the smart switching processing unit circuit using Proteus software package.

Figure (9) shows a flowchart describing the per phase smart switching algorithm which means that this algorithm is repeated for each phase under enhancement. However, assuming that the main phase under enhancement is V_R, which means that for both half cycles of the cycloconverter output waveform V_o is always equals V_R except within the comparison time period (T_C=T2-T1) for both positive and negative half cycles.

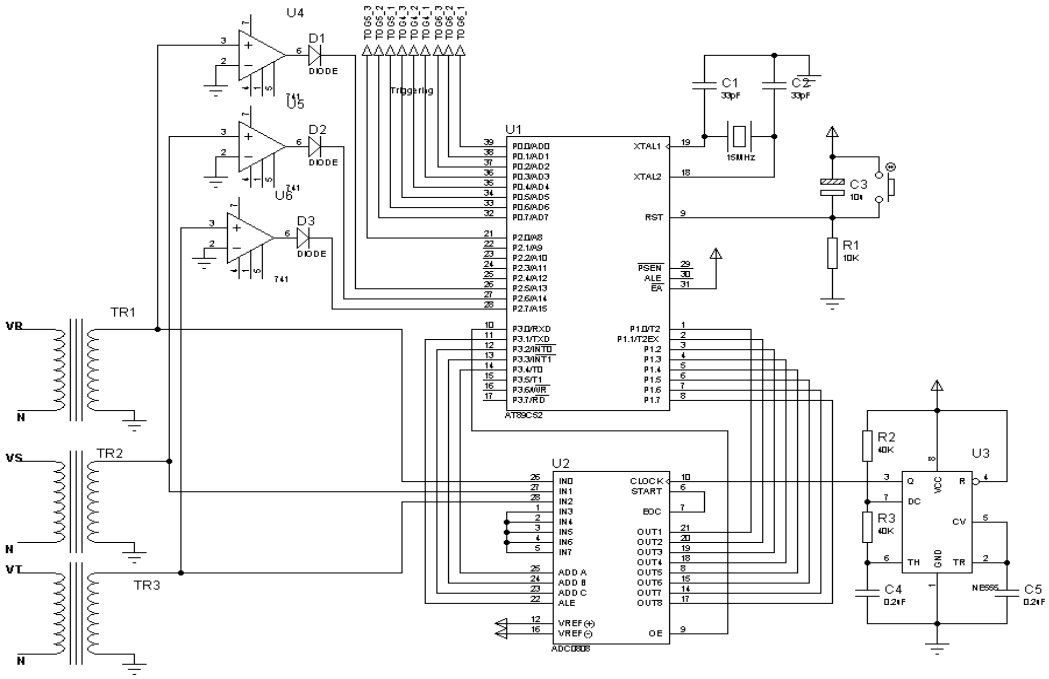


Figure 8: Smart Switching Processor Unit Simulation Circuit

During this comparison period, the processing unit detects the three phases square waveforms converted from the power side and read the instantaneous analogue phase voltages via the 8-bit analogue to digital converter ADC. All together will make the processing unit perform a comparison algorithm within the comparison time period by comparing the magnitude of the main phase (assumed for instant as V_R) with magnitude of other two phases V_S and V_T and accordingly triggering the proper bidirectional switches to switch between phases.

SIMULATION RESULTS

Three phase enhanced waveforms were generated for each divide-by factor (N) to produce waveforms with desired fundamental frequency component with reduced THD%. Figure (10) shows the resultant normalized output waveforms V_{OR}, V_{OS}, and V_{OT} of the proposed system for three cases of the divide-by factor which corresponds to 25Hz, 16.6Hz, and 12.5 Hz generation. The waveforms, unlike these were generated by the ordinary envelope cycloconverter, are smoother and approaching sinusoidal shape.

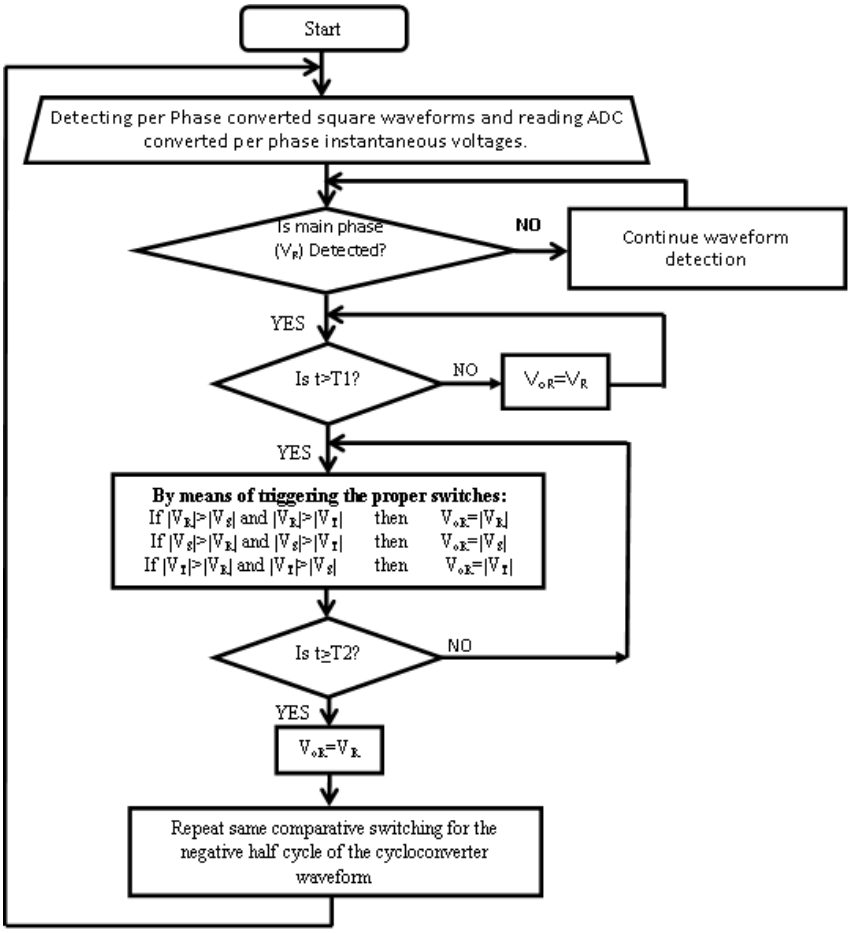


Figure 9: Flowchart Showing the Per Phase Smart Switching Algorithm

To show the improvement in harmonic content, the THD% was calculated for each waveform of each generating frequency case from the frequency spectrum of the output waveform. Moreover, the improvement may be shown by displaying the normalized magnitude of frequency components (C_n) as shown in Figure 11 where the frequency spectrum of three cases of generating fundamental frequency is displayed. The desired frequency component here is the fundamental one which is the dominant and first component.

Phase relations may be also investigated for the three phase output waveforms. The phase relations are displayed for the fundamental and the most nearest harmonic components which are in each case the third and fifth components as shown in Figure 12.

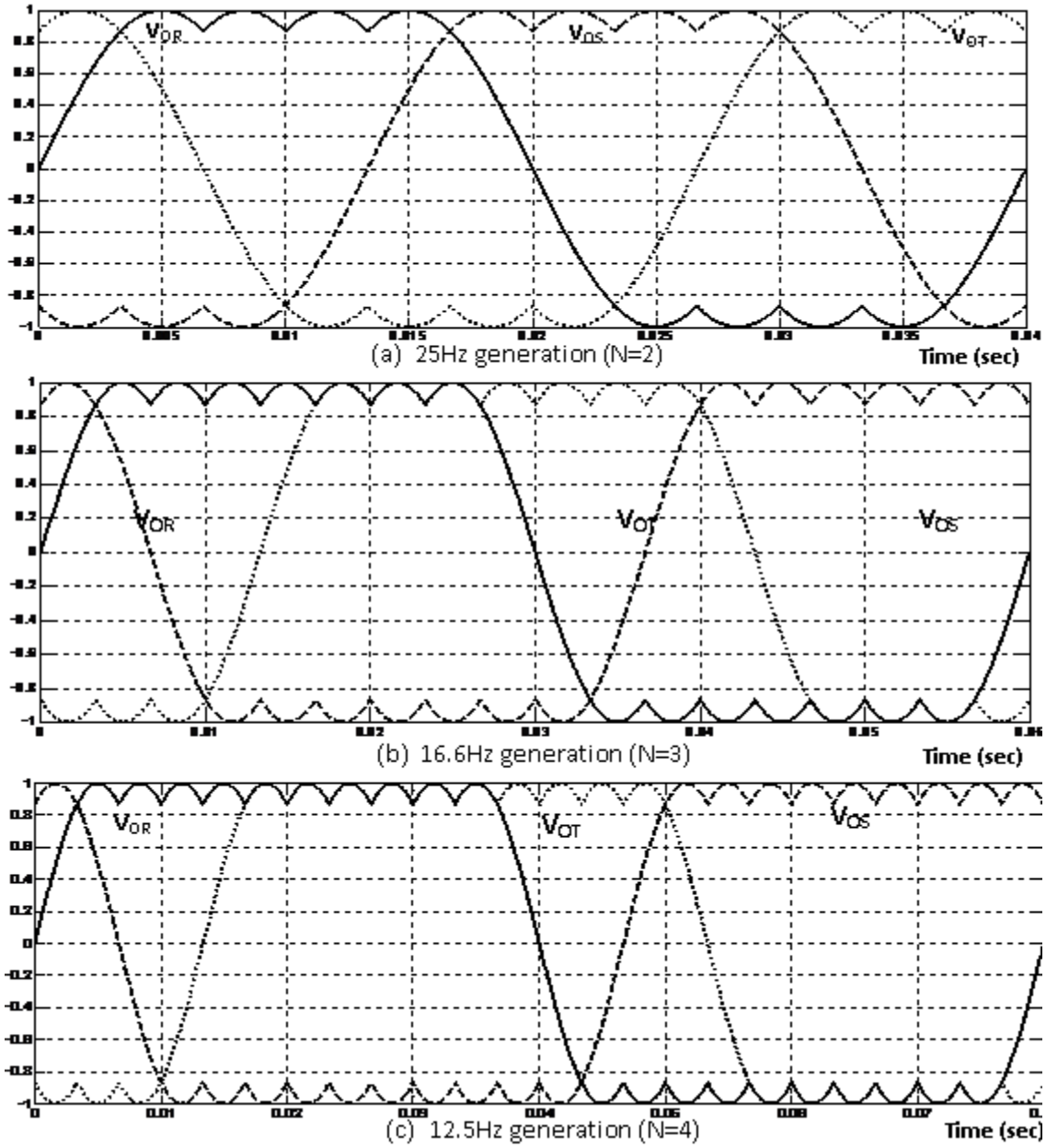


Figure 10: Enhanced Three Phase Output Waveforms

The phase relations between the output waveforms show a balanced fundamental frequency component for the 25Hz generation. Other cases (the 16.6Hz and 12.5Hz) were found almost balanced and all are in same anti-clock wise phase rotation sequence.

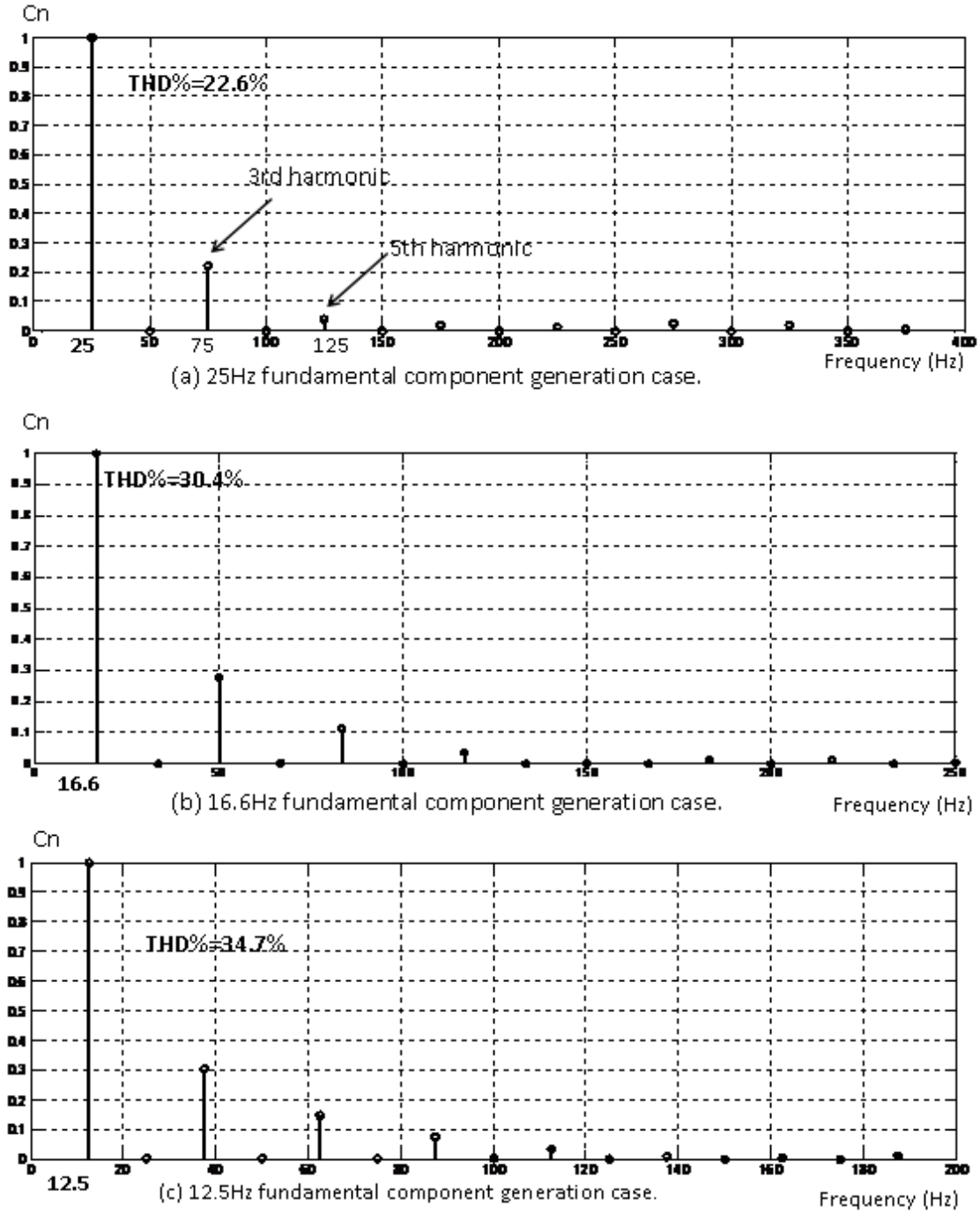


Figure 11: Proposed System Output Waveforms Frequency Spectrum

To show enhancement in THD% criterion for the proposed work, a simple comparison was made of the THD% between the new smart switching technique of phases and the ordinary envelope cycloconverter as shown in Figure 13 where a five desired fundamental frequency generation were considered. This comparison of these cases shows that the proposed system reduces the THD% about 60% of the basic envelope cycloconver.

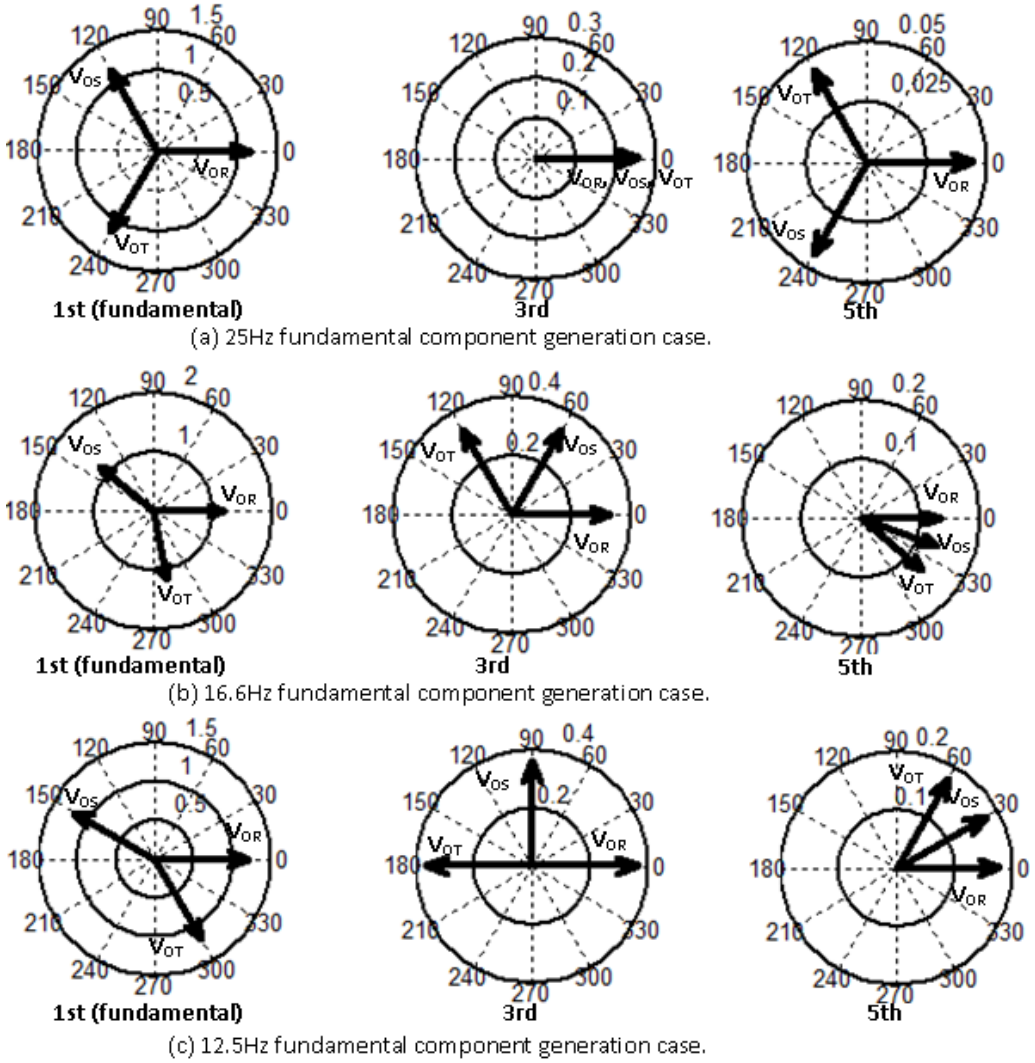


Figure 12: Three Phase Output Waveforms Phase Relations

Figure 13: THD% Comparison between Proposed Work and Ordinary cycloconverter

CONCLUSIONS

The proposed system was found to provide enhanced three phase output waveforms compared to the ordinary cycloconverter output due to its effective reduction in THD% (about 60% reduction) maintaining the basic property of AC-to-AC converters; simplicity and low cost. The proposed system uses processing unit that detect and reads continuously

analogue phase voltages and perform power switching accordingly which gives the additional task of phase failure detection to stop power supplying three phase load. Finally, the proposed system may be considered very useful in low cost requirement applications with acceptable harmonic distortion waveforms where harm harmonic components (3rd and 5^{th}) are reduced compared to the fundamental one.

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